FIG. 1

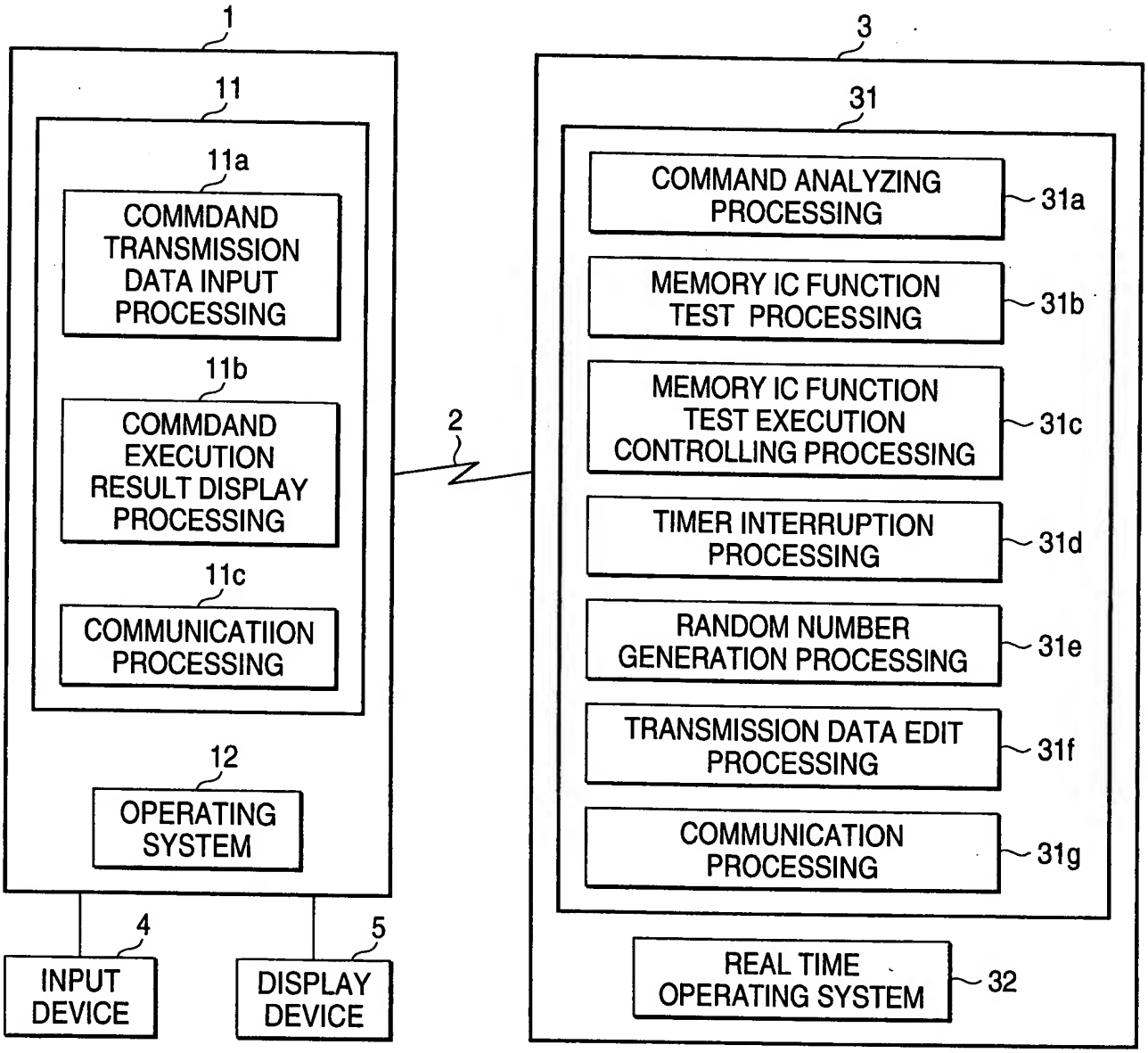

1
11
11a
COMMDAND TRANSMISSION DATA INPUT PROCESSING
11b
COMMDAND EXECUTION RESULT DISPLAY PROCESSING
11c
COMMUNICATIION PROCESSING
12
OPERATING SYSTEM
2
3
31
COMMAND ANALYZING PROCESSING
31a
MEMORY IC FUNCTION TEST PROCESSING
31b
MEMORY IC FUNCTION TEST EXECUTION CONTROLLING PROCESSING
31c
TIMER INTERRUPTION PROCESSING
31d
RANDOM NUMBER GENERATION PROCESSING
31e
TRANSMISSION DATA EDIT PROCESSING
31f
COMMUNICATION PROCESSING
31g
REAL TIME OPERATING SYSTEM
32
4
INPUT DEVICE
5
DISPLAY DEVICE

FIG. 2

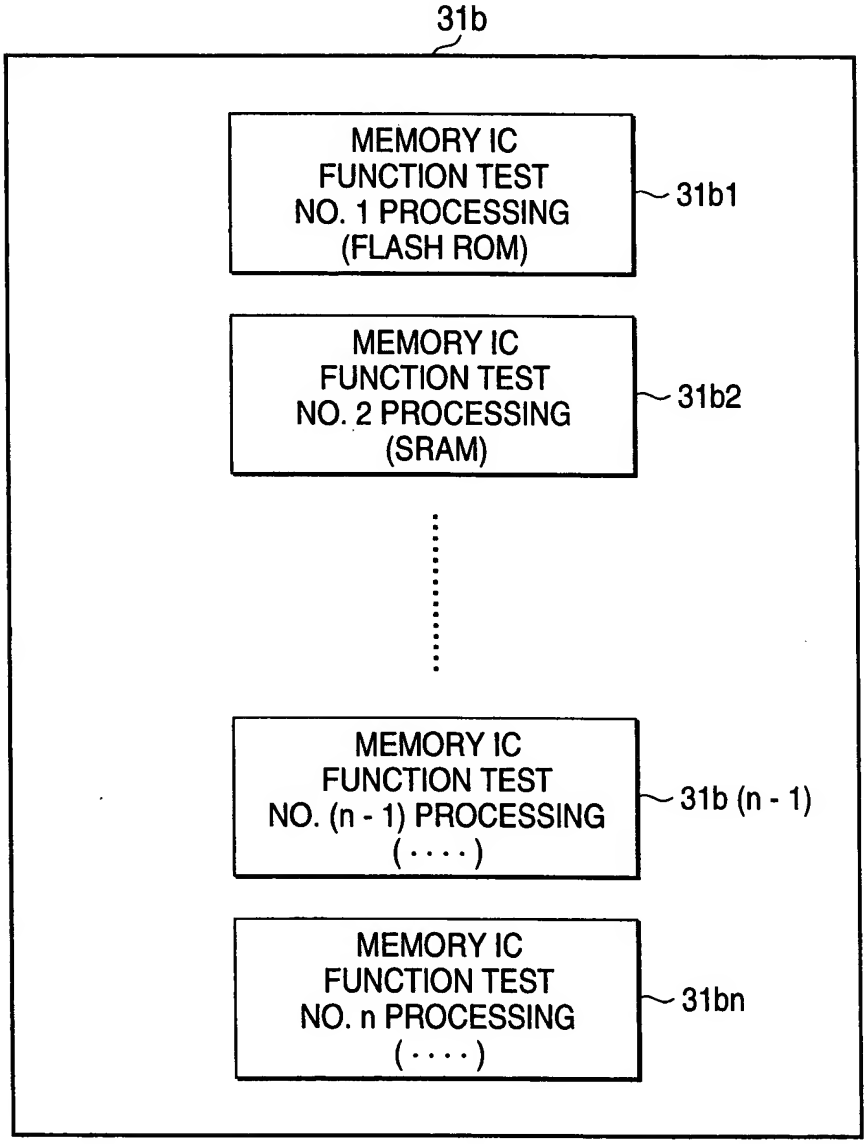

31b
MEMORY IC FUNCTION TEST NO. 1 PROCESSING (FLASH ROM)
31b1
MEMORY IC FUNCTION TEST NO. 2 PROCESSING (SRAM)
31b2
MEMORY IC FUNCTION TEST NO. (n - 1) PROCESSING (· · · ·)
31b (n - 1)
MEMORY IC FUNCTION TEST NO. n PROCESSING (· · · ·)
31bn

FIG. 3

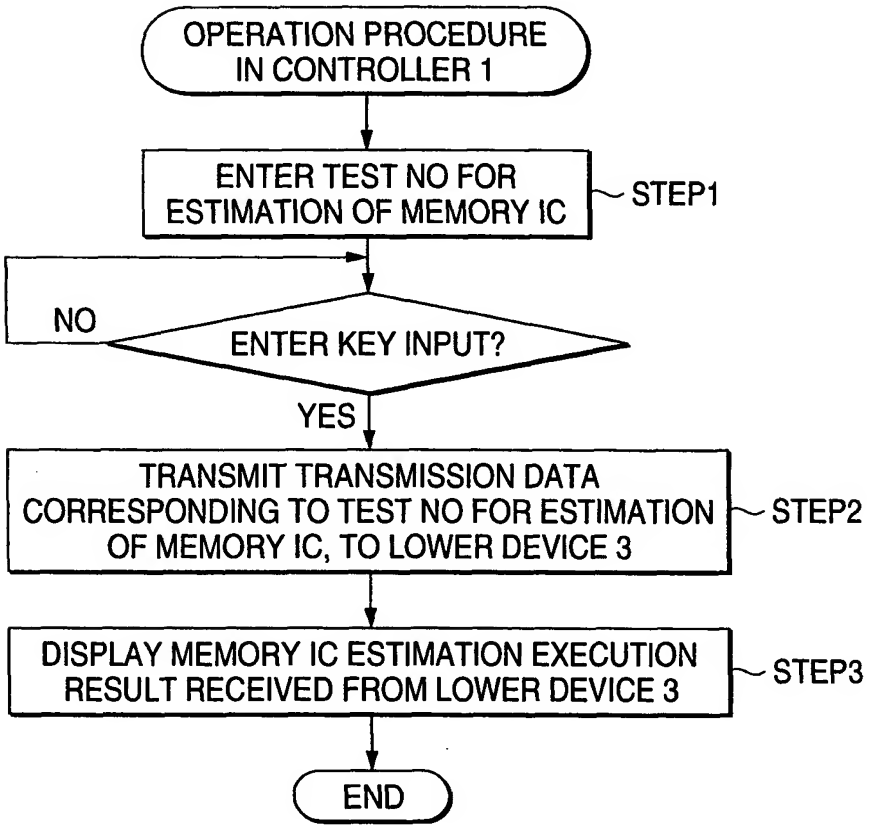

OPERATION PROCEDURE IN CONTROLLER 1
ENTER TEST NO FOR ESTIMATION OF MEMORY IC
STEP1
NO
ENTER KEY INPUT?
YES
TRANSMIT TRANSMISSION DATA CORRESPONDING TO TEST NO FOR ESTIMATION OF MEMORY IC, TO LOWER DEVICE 3
STEP2
DISPLAY MEMORY IC ESTIMATION EXECUTION RESULT RECEIVED FROM LOWER DEVICE 3
STEP3
END

FIG. 4

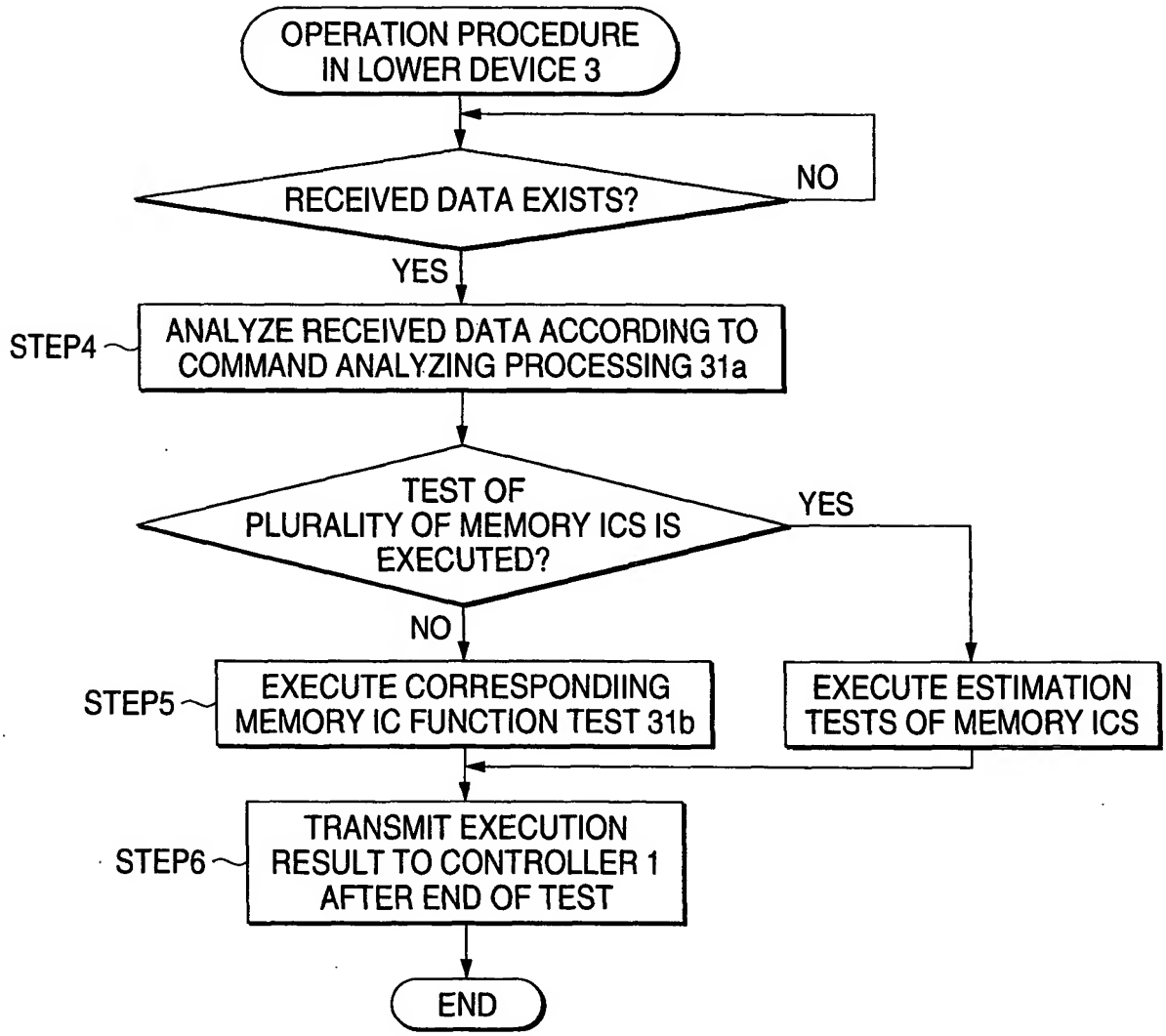

OPERATION PROCEDURE IN LOWER DEVICE 3
RECEIVED DATA EXISTS?
NO
YES
STEP4
ANALYZE RECEIVED DATA ACCORDING TO COMMAND ANALYZING PROCESSING 31a
TEST OF PLURALITY OF MEMORY ICS IS EXECUTED?
YES
NO
STEP5
EXECUTE CORRESPONDIING MEMORY IC FUNCTION TEST 31b
EXECUTE ESTIMATION TESTS OF MEMORY ICS
STEP6
TRANSMIT EXECUTION RESULT TO CONTROLLER 1 AFTER END OF TEST
END

FIG. 5

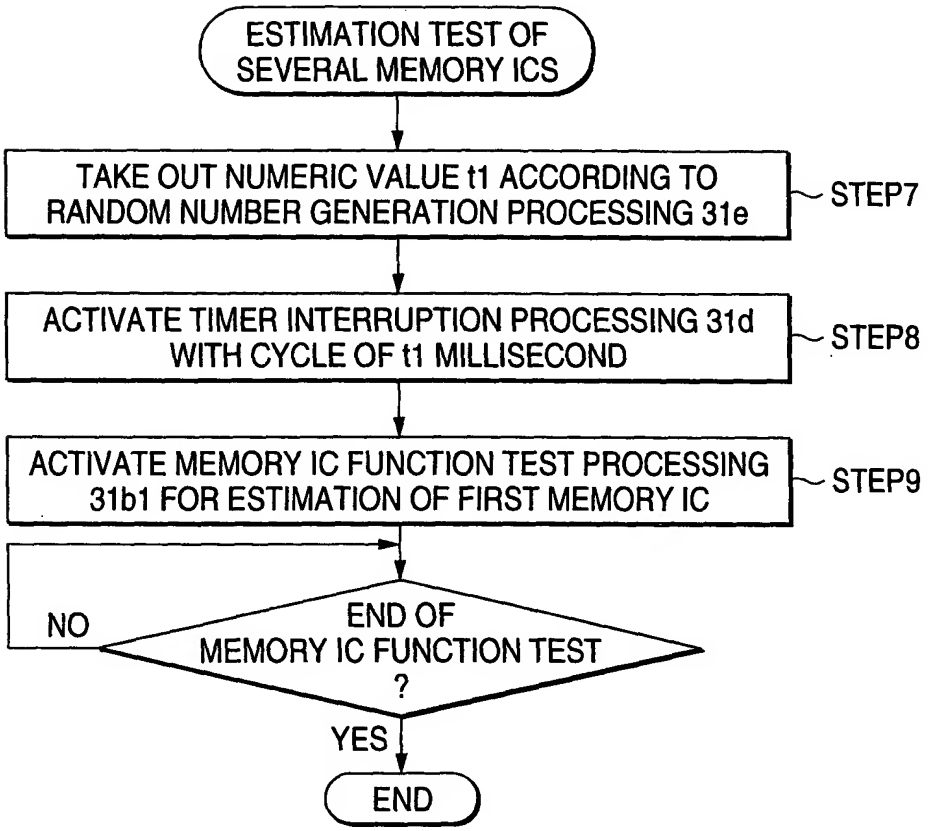

ESTIMATION TEST OF SEVERAL MEMORY ICS
TAKE OUT NUMERIC VALUE t1 ACCORDING TO RANDOM NUMBER GENERATION PROCESSING 31e
STEP7
ACTIVATE TIMER INTERRUPTION PROCESSING 31d WITH CYCLE OF t1 MILLISECOND
STEP8
ACTIVATE MEMORY IC FUNCTION TEST PROCESSING 31b1 FOR ESTIMATION OF FIRST MEMORY IC
STEP9
NO
END OF MEMORY IC FUNCTION TEST ?
YES
END

FIG. 6

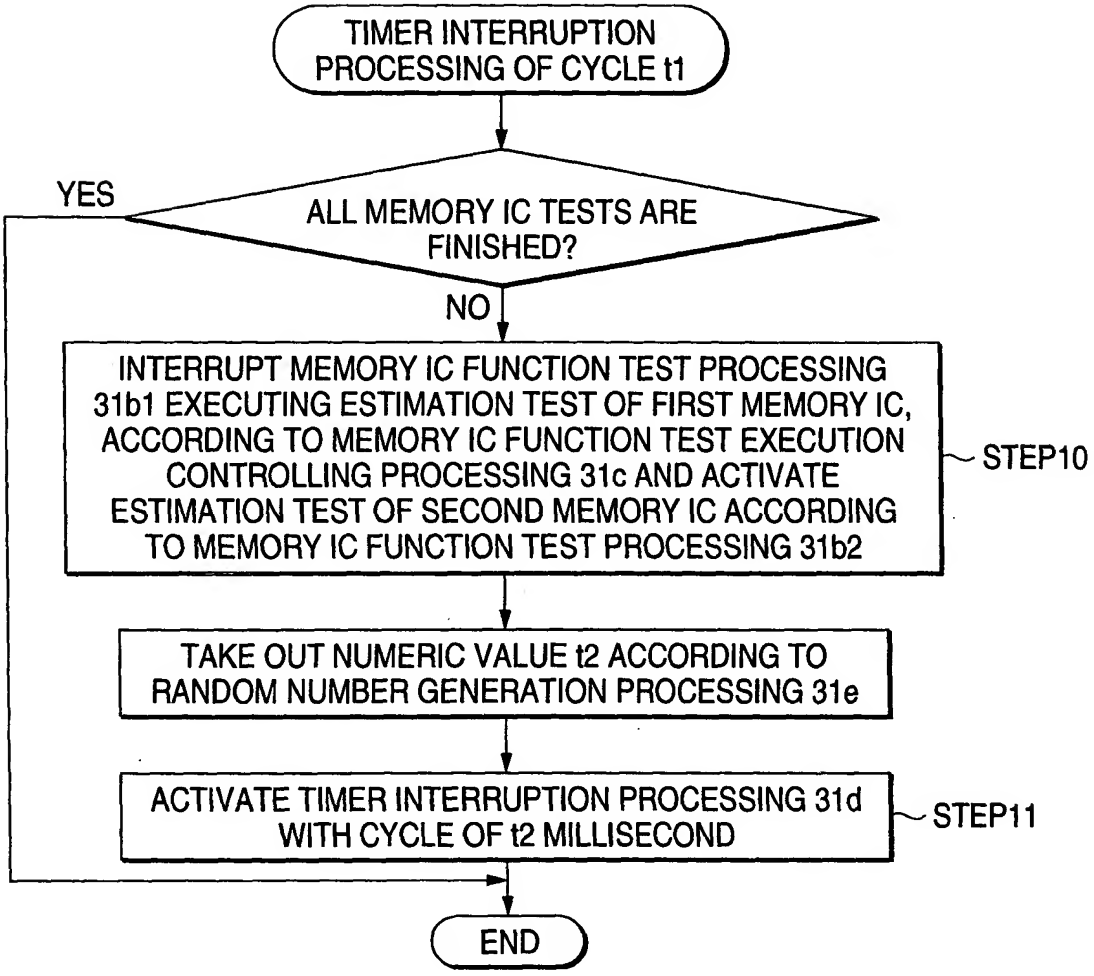

TIMER INTERRUPTION PROCESSING OF CYCLE t1
YES
ALL MEMORY IC TESTS ARE FINISHED?
NO
INTERRUPT MEMORY IC FUNCTION TEST PROCESSING 31b1 EXECUTING ESTIMATION TEST OF FIRST MEMORY IC, ACCORDING TO MEMORY IC FUNCTION TEST EXECUTION CONTROLLING PROCESSING 31c AND ACTIVATE ESTIMATION TEST OF SECOND MEMORY IC ACCORDING TO MEMORY IC FUNCTION TEST PROCESSING 31b2
STEP10
TAKE OUT NUMERIC VALUE t2 ACCORDING TO RANDOM NUMBER GENERATION PROCESSING 31e
ACTIVATE TIMER INTERRUPTION PROCESSING 31d WITH CYCLE OF t2 MILLISECOND
STEP11
END

FIG. 7

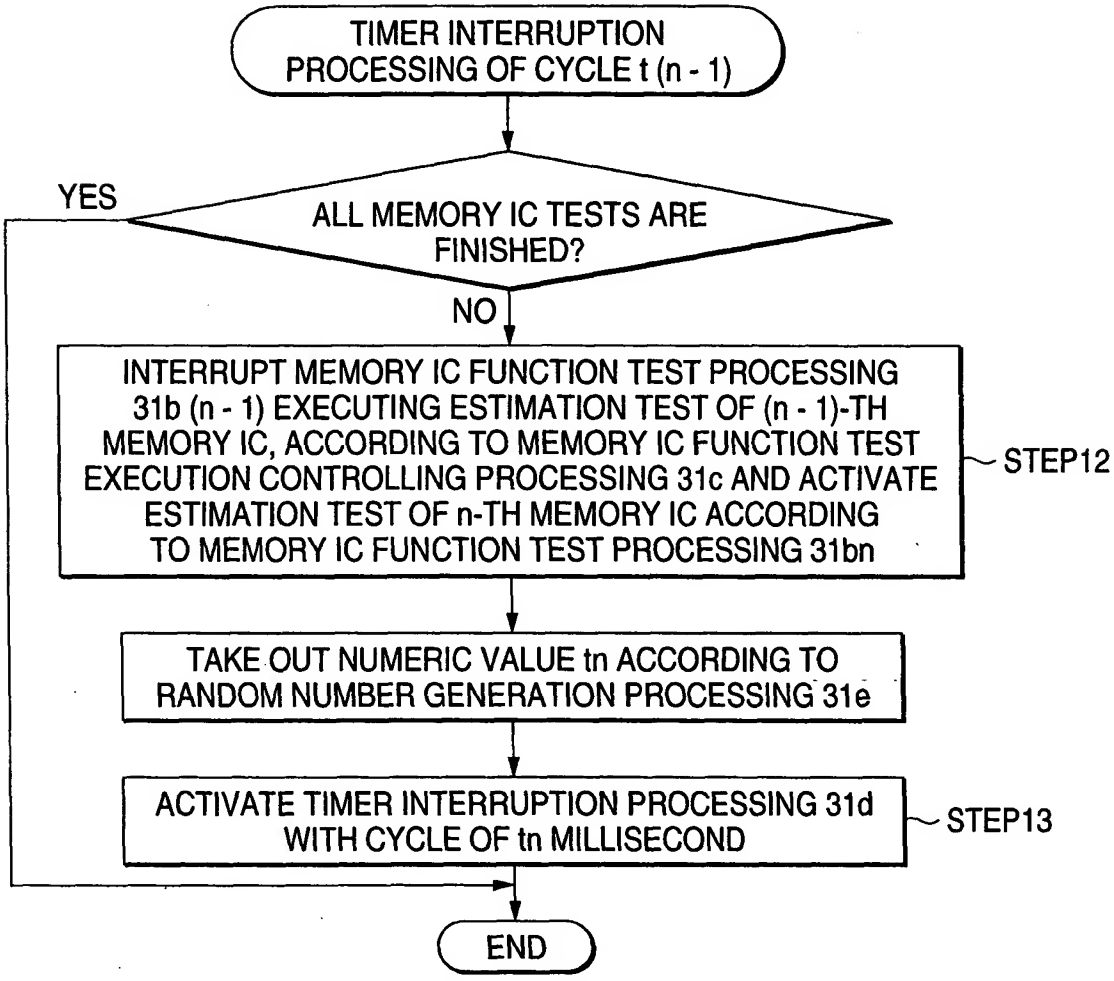
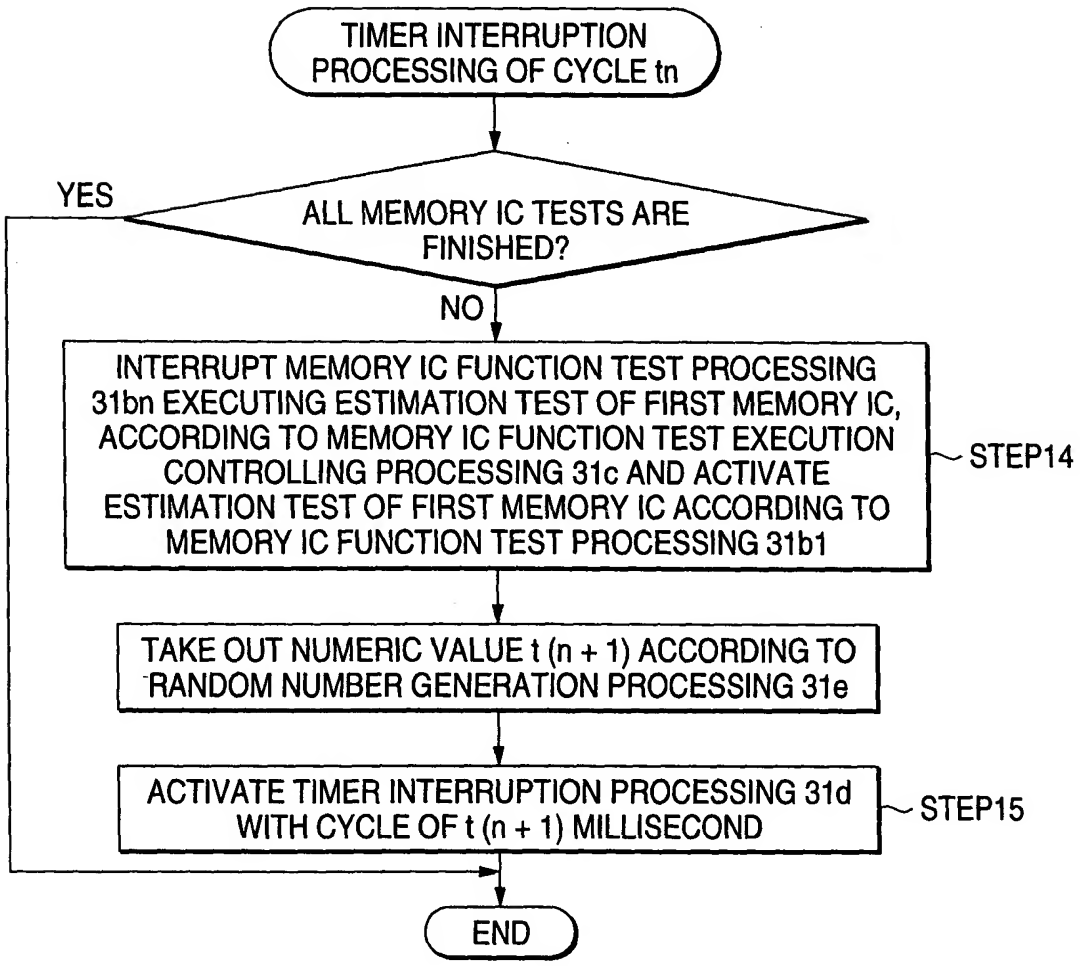

TIMER INTERRUPTION PROCESSING OF CYCLE t (n - 1)
YES
ALL MEMORY IC TESTS ARE FINISHED?
NO
INTERRUPT MEMORY IC FUNCTION TEST PROCESSING 31b (n - 1) EXECUTING ESTIMATION TEST OF (n - 1)-TH MEMORY IC, ACCORDING TO MEMORY IC FUNCTION TEST EXECUTION CONTROLLING PROCESSING 31c AND ACTIVATE ESTIMATION TEST OF n-TH MEMORY IC ACCORDING TO MEMORY IC FUNCTION TEST PROCESSING 31bn
STEP12
TAKE OUT NUMERIC VALUE tn ACCORDING TO RANDOM NUMBER GENERATION PROCESSING 31e
ACTIVATE TIMER INTERRUPTION PROCESSING 31d WITH CYCLE OF tn MILLISECOND
STEP13
END

FIG. 8


TIMER INTERRUPTION PROCESSING OF CYCLE tn
YES
ALL MEMORY IC TESTS ARE FINISHED?
NO
INTERRUPT MEMORY IC FUNCTION TEST PROCESSING 31bn EXECUTING ESTIMATION TEST OF FIRST MEMORY IC, ACCORDING TO MEMORY IC FUNCTION TEST EXECUTION CONTROLLING PROCESSING 31c AND ACTIVATE ESTIMATION TEST OF FIRST MEMORY IC ACCORDING TO MEMORY IC FUNCTION TEST PROCESSING 31b1
STEP14
TAKE OUT NUMERIC VALUE t (n + 1) ACCORDING TO RANDOM NUMBER GENERATION PROCESSING 31e
ACTIVATE TIMER INTERRUPTION PROCESSING 31d WITH CYCLE OF t (n + 1) MILLISECOND
STEP15
END

>sram, t1, paXXXXXXX, pbXXXXXXX, pc4, pe1, pg1, ph1, pi1 ↓ ↓
SRAM test start
>sdram, t1, paXXXXXXX, pbXXXXXXX, pc4, pe1, pg1, ph1, pi1 ↓ ↓
SDRAM test start
EXECUTE THE SRAM TEST 1 (W/R/C TEST) UNDER THE FOLLOWING CONDITIONS.
pa: ACCESS START ADDRESS
pb: ACCESS END ADDRESS
pc: ACCESS TYPE (1: 8 BITS/2: 16 BITS/3: 32 BITS/4: ALL)
pe: TEST DATA (1: INCREMENT DATA/2: FIXED DATA)
pg: EXECUTION TIME, ONCE
ph: THERE IS/ISN'T DISPLAY DURING EXECUTION (1: NO DIAPLAY/2: DISPLAY)
pi: OPERATION IN THE EVENT OF ERROR GENERATION (1: STOP/2: CONTINUE)
EXECUTE THE SDRAM TEST 1 (W/R/C TEST) UNDER THE FOLLOWING CONDITIONS.
pa: ACCESS START ADDRESS
pb: ACCESS END ADDRESS
pc: ACCESS TYPE (1: 8 BITS/2: 16 BITS/3: 32 BITS/4: ALL)
pe: TEST DATA (1: INCREMENT DATA/2: FIXED DATA)
pg: EXECUTION TIME, ONCE
ph: THERE IS/ISN'T DISPLAY DURING EXECUTION (1: NO DIAPLAY/2: DISPLAY)
pi: OPERATION IN THE EVENT OF ERROR GENERATION (1: STOP/2: CONTINUE)
UPON RECEIPT OF THE "END" COMMAND DURING THE EXECUTION OF THE TEST,
THE CURRENT EXECUTING TEST IS CANCELLED AND FINISHED.

FIG. 9

FIG. 10

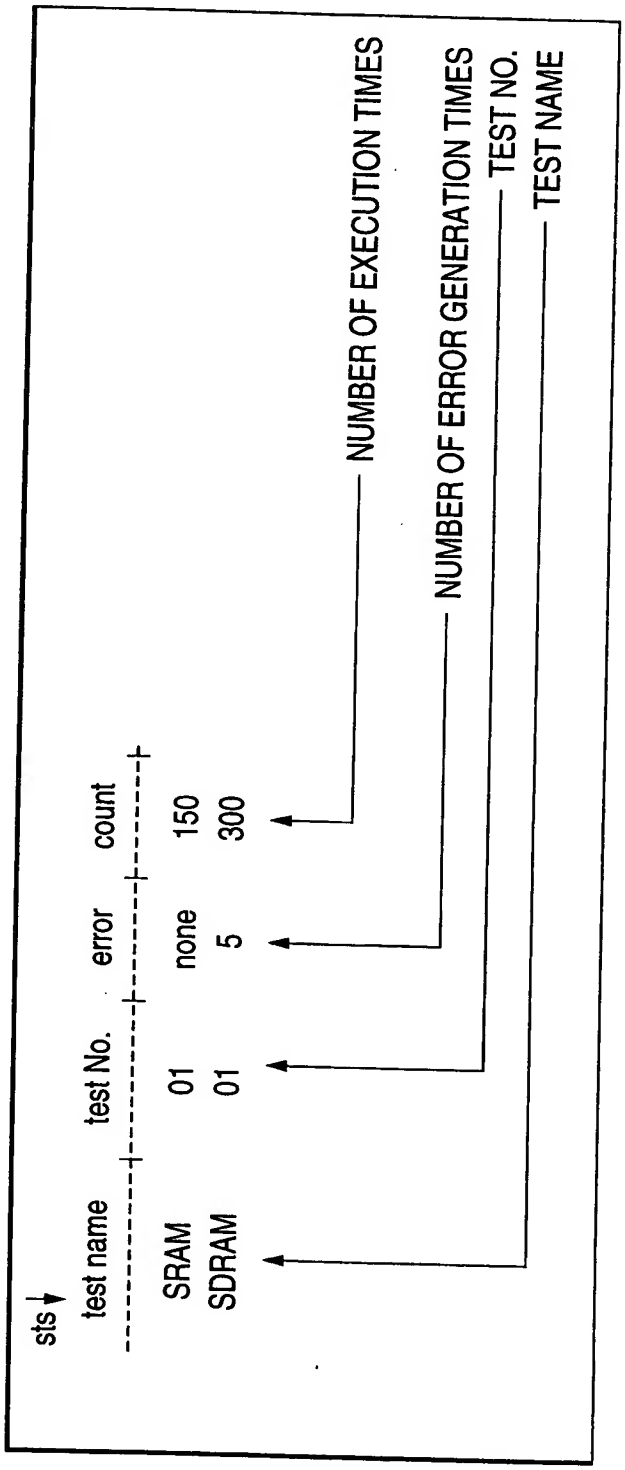

sts
test name
test No.
error
count
SRAM
01
none
150
SDRAM
01
5
300
NUMBER OF EXECUTION TIMES
NUMBER OF ERROR GENERATION TIMES
TEST NO.
TEST NAME

FIG. 11

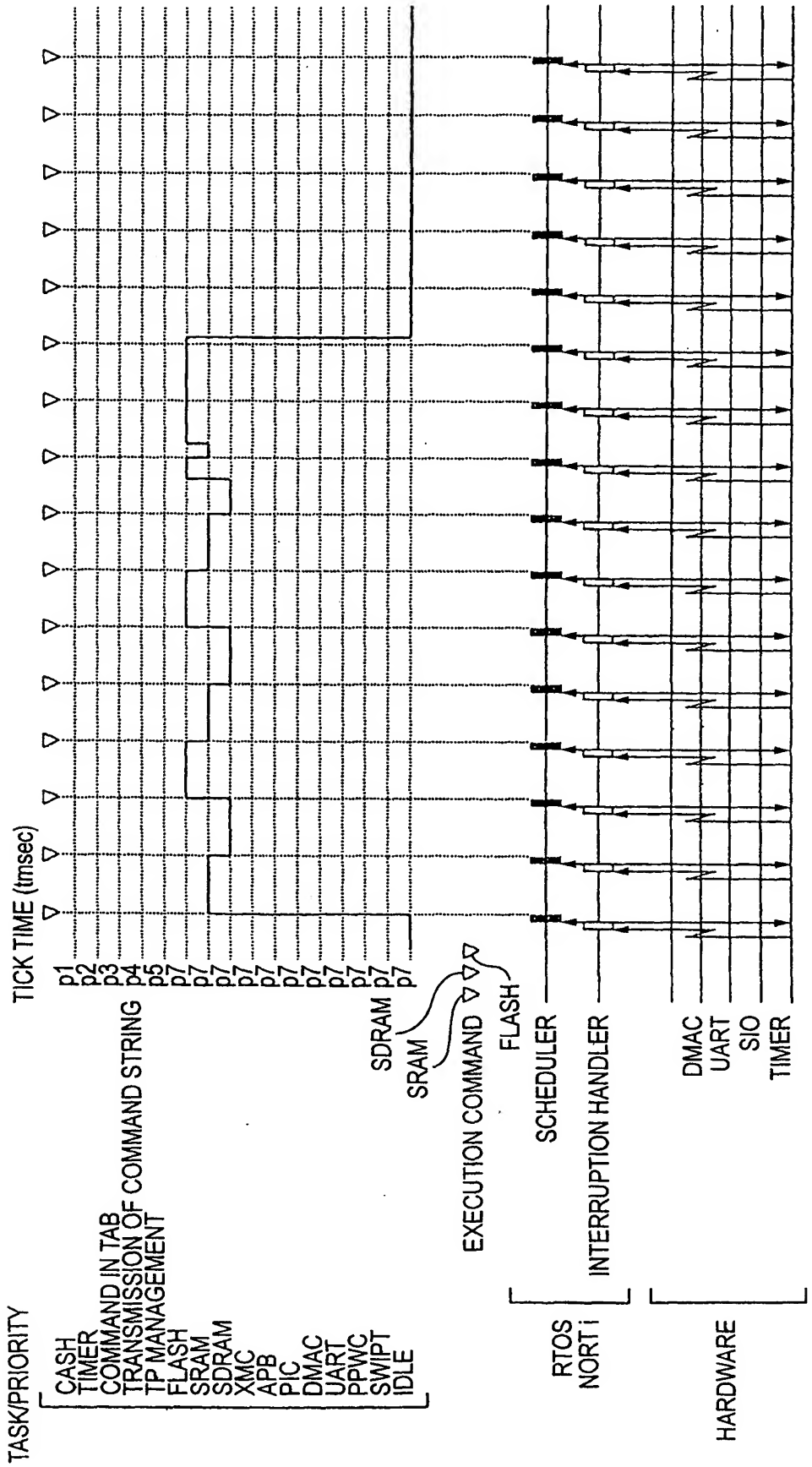
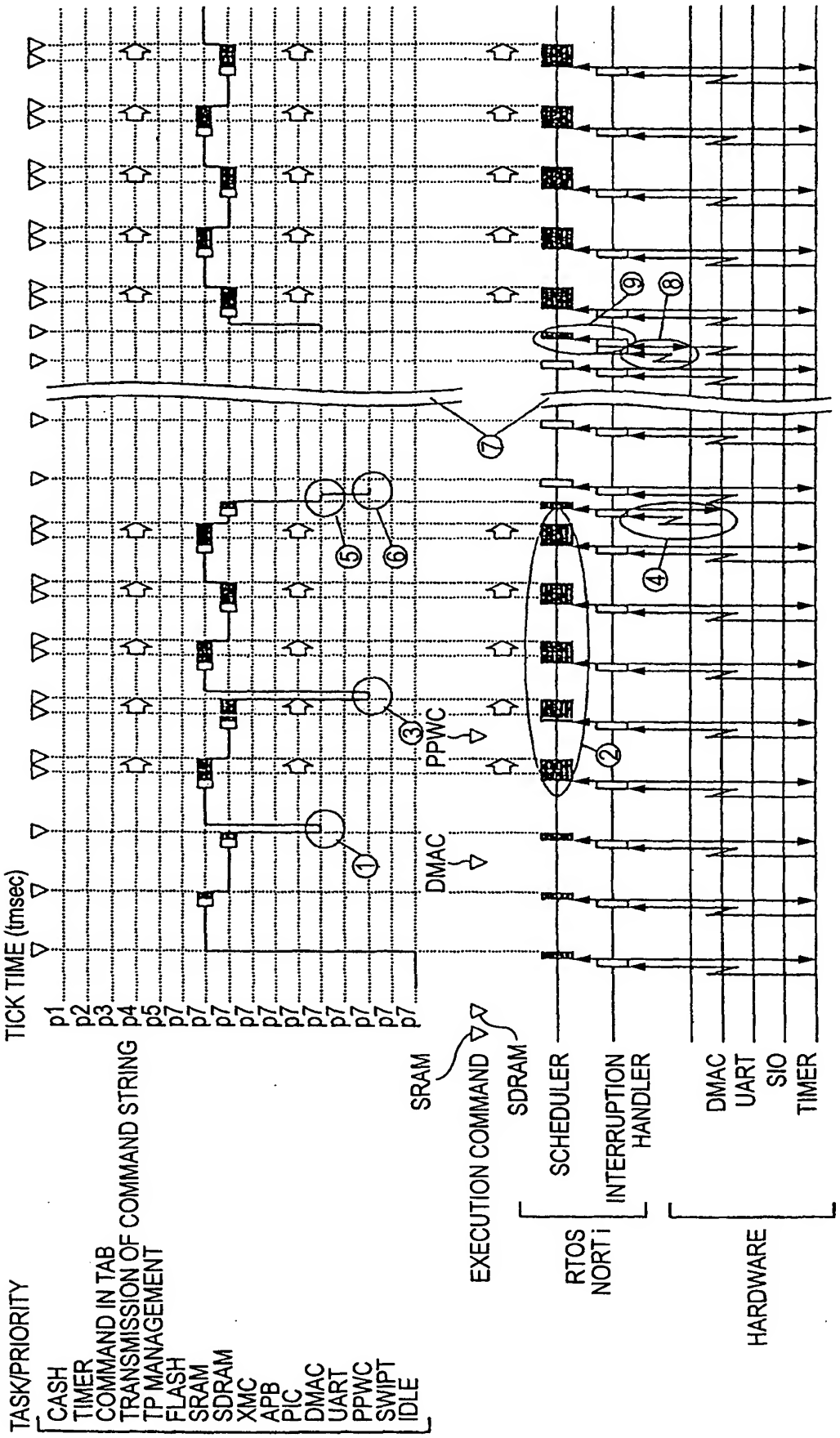

TASK/PRIORITY
CASH
TIMER
COMMAND IN TAB
TRANSMISSION OF COMMAND STRING
TP MANAGEMENT
FLASH
SRAM
SDRAM
XMC
APB
PIC
DMAC
UART
PPWC
SWIPT
IDLE
TICK TIME (tmsec)
p1
p2
p3
p4
p5
p7
SDRAM
SRAM
EXECUTION COMMAND
FLASH
SCHEDULER
INTERRUPTION HANDLER
RTOS NORTi
DMAC
UART
SIO
TIMER
HARDWARE

FIG. 12


TASK/PRIORITY
CASH
TIMER
COMMAND IN TAB
TRANSMISSION OF COMMAND STRING
TP MANAGEMENT
FLASH
SRAM
SDRAM
XMC
APB
PIC
DMAC
UART
PPWC
SWIPT
IDLE
TICK TIME (tmsec)
p1
p2
p3
p4
p5
p7
DMAC
PPWC
SRAM
EXECUTION COMMAND
SDRAM
SCHEDULER
INTERRUPTION HANDLER
RTOS NORTi
DMAC
UART
SIO
TIMER
HARDWARE
①
②
③
④
⑤
⑥
⑦
⑧
⑨